REMARKS

Claims 12-16 and 22-25 are pending, of which claims 22-25 are allowed, and claims 12-16 are under consideration.

Claims 12 and 13 are amended to more clearly describe the preset invention, not to overcome the cited references, and are supported by FIGS. 3A-3L of Applicants' applicaiton.

No new matter is being presented, and for at least the reasons stated below, an allowance of the claims 12-16 is earnestly solicited.

REJECTION UNDER 35 U.S.C. §102(b):

At page 2 of the Office Action, claim 12 was rejected under 35 U.S.C. §102(b) as being anticipated by Yamazaki et al. (US 6,017,783). This rejection is respectfully traversed.

Yamazaki et al. (US) appears to disclose a TFT for a liquid crystal display (LCD) device, having a substrate 1, a gate electrode 8, and an anodic oxidation film 10 which is formed "*around the sidewall of the gate electrode 8*" by immersing the substrate 1 in an electrolytic solution. (See FIG. 1, column 3, lines 29-31, and column 4, lines 1-16.)

However, Yamazaki et al. (US) does not appear to recite every element of the Applicants' claim 12. That is, Yamazaki et al. (US) fails to disclose or suggest, for example, "spacers formed...*on both sidewall portions of said gate electrode and said capping layer*." (Emphasis added.) In other words, with reference to FIG. 3L of Applicants' application, Yamazaki et al. (US) does not explicitly disclose a TFT having spacers 41 which are formed over a first insulating layer 34 and on both sidewall portions of a gate electrode 37 and a capping layer 38.

Additional structural differences illustrate, for example, different methods used to fabricate the respective TFT devices. For example, dashed lines of FIG. 1 of Yamazaki et al. (US) illustrate that source and drain regions 3 are also formed *below the anodic oxidation film/spacer* 10, whereas FIG. 3L shows and claim 12 recites, that *high-density* source and drain regions 44-1 and 44-2 are "formed at the ones of the end portions of said semiconductor layer exposed *beyond said spacers*." (Emphasis added.)

In order for a document to anticipate a claim, the document must teach each and every element of the claim. See MPEP §2131. Accordingly, since Yamazaki et al. (US) does not teach the features recited in independent claim 12, as stated above, withdrawal of the § 102(a) rejection is earnestly solicited.

REJECTION UNDER 35 U.S.C. §103(a):

At pages 3 and 4 of the Office Action, claims 12, 13, 15 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki et al. (JP 11-261076) in view of Uchida et al. (JP 5-121435). At pages 3, 4 and 5 of the Office Action, claims 13 and 14 were further rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki et al. (U.S.) in view of Liang et al. (US 6,071,783). These rejections are overcome in view of the following arguments. Accordingly, withdrawal of the rejections is respectfully requested.

Yamazaki et al. (JP) in view of Uchida et al.:

At this time, Applicants respectfully submit that the Patent Office has not met the burden to provide evidence to support an obviousness rejection. That is, the Examiner has not substantiated elements shown in FIG. 13 of Yamazaki et al. (JP) supporting that, for example, an element 2110 is a capping layer, apart from the unsubstantiated assertions of the Examiner. In fact, the abstract of Yamazaki et al. (JP) explicitly discloses the element 2110 as a metal layer of the gate electrode 2000, and not "a capping layer formed over said gate electrode," as asserted by the Examiner. It is now well established that all claim limitations must be taught or suggested in prior art references, and that an evidence or document, must be presented to show elements recited in the Applicants' claims. (See In re Zurko, 258, F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001)).

Assuming arguendo that Yamazaki et al. (JP) discloses a transistor having a substrate 1000, a semiconductor layer 1130, a first insulating layer 1200 formed over the semiconductor layer 1130, and a gate electrode 2000 formed over the first insulating layer 1200, Applicants' respectfully note that Yamazaki et al. (JP) fails to disclose or suggest many of the other elements recited in claim 12.

For example, in addition to failing to disclose a structure where source and drain electrodes are formed to directly contact respective high-density source and drain regions, Yamazaki et al. (JP) fails to disclose or suggest a TFT having "spacers formed *over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer*," as recited in claim 12. (Emphasis added.) In contrast, FIG. 13 and abstract of Yamazaki et al. (JP) disclose either an oxide layer 2210 which is formed between the first insulating layer 1200 and the metal layer 2110, or an insulating film 1300 which surrounds the gate electrode 2000 and is level with the first insulating layer 1200.

Applicants respectfully submit that Uchida et al. does not supplement the missing elements in Yamazaki et al. (JP). Furthermore, Applicants respectfully note that the cited references do not provide 1) a motivation to combine and 2) a reasonable expectation of success thereof, as required by the §103(a) rejection.

Uchida et al. appears to disclose a TFT having a substrate 7, a gate electrode 3 formed over the substrate 7, a first insulating layer 6 formed on the substrate 7 to bury the gate electrode 3, a semiconductor layer 7 formed over the first insulating layer 6, and a passivation film 8 patterned over the semiconductor layer 7. (See FIG. 3(d2) and Abstract.)

Again, assuming reference numerals 11 and 12 refer to source and drain electrodes, and 9 refers to high-density source and drain regions, Applicants note that in FIG. 3(d2) of Uchida et al., the gate electrode 3 is formed below the semiconductor layer 7, whereas in FIG. 13 of Yamazaki et al. (JP), the gate electrode 2000 is formed on top of the semiconductor layer 1130. In short, Yamazaki et al. (JP) and Uchida et al. disclose TFT devices having very different structures, and accordingly, quite different fabrication technologies thereof. That is, the references themselves do not provide a motivation to make such necessary modification to arrive at the present invention. Applicants note that to even consider such a modification, for example, to provide Yamazaki et al. (JP) with structures of Uchida et al. (source and drain electrodes that directly contact source and drain regions), complete new engineering decisions are required, which certainly are not supported by the disclosures of Yamazaki et al.,(JP) and Uchida et al.

The Board has repeatedly held that a finding of obviousness requires that the prior art provide a motivation for one skilled in the art to make the necessary changes to the reference device. In other words, Applicants' disclosure may not be used as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention. (See, e.g., In re Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. Pat. App. 1984) and MPEP §§ 2141-2142.) These findings were upheld *even where the references relied upon teach that all aspects of the claimed invention were individually known in the art.* (See, e.g., Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).)

With respect to claims 13, 15 and 16, although the Examiner asserts elements 107 and 108 of FIG. 1 of Yamazaki et al. (JP) are "low-density source and drain regions having a same conductivity as said high-density source and drain regions...wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers," and an element 105/105a is a

"silicide layer," the Examiner has not specifically pointed out where these disclosures are made in Yamazaki et al. (JP), which is in the Japanese language. Applicants respectfully note that the English abstract of Yamazaki et al. (JP) also does not support the Examiner assertion, and it is inappropriate for the Examiner to second guess and define the elements himself/herself.

Regarding the use of foreign language abstracts/publications, the court in Ex parte Gavin noted: "[i]n this appeal, the examiner relied upon abstracts of two published Japanese patent applications without referring to translations of the underlying applications...[abstracts do] not incorporate by reference any disclosure of the underlying document...in virtually all cases, they are incomplete." (Ex parte Gavin, 62 USPQ2d 1680, 1683 (BPAI 2001).) "Generally an abstract does not provide enough information to permit an objective evaluation of the validity of what it describes...It is our opinion that a proper examination under 37 CFR §1.104 should be based on the underlying documents and translations, where needed. Accordingly, the preferred practice is for the examiner to cite and rely on the underlying document." (Emphasis added, Id. at 1684.)

In short, courts have held that reliance on abstracts of the cited foreign language reference to both disclose all the claimed features and the purported motivation or suggestion for their combination is improper. As noted above, the outstanding rejection is based primarily on elements cited in the figures, which are not even mentioned in the abstracts of two Japanese language references. Since a proper understanding of what each reference discloses can only be found through a translation of each reference, Applicants respectfully request translations of Yamazaki et al. (JP) and Uchida et al. be provided in any future Office Action relying on the same.

Yamazaki et al. (U.S.) in view of Liang et al.:

With respect to claims 13 and 14, Applicants have already shown above that Yamazaki et al. (US) fails to disclose or suggest a TFT having "spacers formed *over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer*," as recited in claim 12. (Emphasis added.) As admitted by the Examiner, Yamazaki et al. (US) also fails to disclose or suggest having "low-density source and drain regions...formed at regions of said semiconductor layer and said spacers, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers." Applicants note Liang et al. does not supplement the missing elements in Yamazaki et al. (US). Furthermore, Applicants respectfully submit that the cited references in this rejection also do not provide 1) a motivation to combine and 2) a reasonable expectation of success thereof, as required by the §103(a) rejection.

The prior art must not only suggest the desirability that the teachings of references be combined, but must also suggest the desirability of the modification in the manner proposed by the Examiner as well as the result to be achieved. (See Diversitech v. Century Steps, 850 F.2d 675, 7 USPQ.2d 1315 (Fed. Cir. 1988).) In the instant case, the cited references do not meet the above requirements, and therefore, it is respectfully submitted that the 103(a) rejection cannot be supported in the instant case.

While the Examiner appears to cast the present invention as a combination of old elements, for example, by adding lightly doped source/drain regions 6b and 6c of a semiconductor layer 1 of a MOSFET device of Liang et al. (FIG. 8), to a semiconductor layer 1 of a TFT device of Yamazaki et al. (US) (FIG. 1) having a completely different structure, this leads to an improper analysis of the present invention by parts and not by the whole. This is well established in view of Custom Accessories, Inc. v. Jeffery-Allan Industries, Inc., 807 F.2d 955, 1 USPQ.2d 1196 (Fed. Cir. 1986).

Additionally, even if such a motivation exist, it appears that such a modification would require complete new engineering decisions, and the cited references certainly do not provide a reasonable expectation of success thereof. That is, Applicant respectfully notes that the fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness, and the teaching or suggestion to make the claimed combination and the reasonable expectation of success, must both be found in the prior art, and not based on applicant's disclosure. (See MPEP § 2143.)

It is also well established that the Examiner may not rely on general principles of engineering to fill in the gaps in the teaching of the cited references. (See Akzo v. Dupont, 810 F.2d 1148, 1 USPQ.2d 1704 (Fed. Cir. 1987).) Applicant respectfully submits that the cited references do not disclose a motivation to combine, and a reasonable expectation of success of what is claimed in the present invention.

In view of the above, Applicants believe that independent claim 12 is patentably distinguishable over the cited references, and withdrawal of the § 103(a) rejection is respectfully requested. In addition, claims 13-16 are allowable at least due to their dependency on claim 12, as well as for the additional features recited therein, and withdrawal of the §103(a) rejection for these claims is also respectfully requested.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please AMEND claims 12 and 13 as follows. For the convenience of the Examiner, all pending claims 12-16 and 22-25 are presented herein below:

12. (ONCE AMENDED) A thin film transistor (TFT), comprising:

a substrate;

a semiconductor layer formed over said substrate having end portions;

a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer;

a gate electrode formed over said first insulating layer;

a capping layer formed over said gate electrode;

spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer;

high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; and

source and drain electrodes which directly contact, respectively, said high density source and drain regions.

13. (ONCE AMENDED) The TFT of claim 12, further comprising low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers.

14. (UNAMENDED) The TFT of claim 12, wherein said first insulating layer, said capping layer and said spacer are one of an oxide layer and a nitride layer.

15. (UNAMENDED) The TFT of claim 12, further comprising a silicide layer formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

16. (UNAMENDED) The TFT of claim 15, wherein said silicide layer is of a refractory metal.

22. (UNAMENDED) An active matrix display device, comprising:

a substrate;

a semiconductor layer having end portions formed over said substrate;

a first insulating layer formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer;

a gate electrode formed over said first insulating layer;

a capping layer formed over said gate electrode;

spacers formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer;

high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers;

source and drain electrodes which directly contact, respectively, said high density source and drain regions;

a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes; and

a pixel electrode formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion.

23. (UNAMENDED) The active matrix display device of claim 22, further comprising low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers.

24. (UNAMENDED) The active matrix display device of claim 22, further comprising silicide layers formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

25. (UNAMENDED) The active matrix display device of claim 22, further comprising an organic electro-luminescence (EL) layer and a cathode electrode sequentially formed on a first predetermined area of said pixel electrode and on a second predetermined area of said planarization layer.